REMARKS

The Office Action dated October 21, 2002 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. By this Amendment, claim 18 has been canceled without prejudice or disclaimer, and claims 1, 4, 7 and 12 have been amended to more clearly point out and distinctly claim the invention. No new matter has been added. Accordingly, claims 1-17 are now pending in this application and submitted for consideration.

Section 112 Rejection

Claim 18 is rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification.

This rejection is now moot in view of cancellation to claim 18.

Section 103 Rejection

Claims 1-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Maruyama et al. (US Patent Pub. No. 2001/0003199, hereinafter "Maruyama") in view of Dye (U.S. Patent No. 6,173,381).

As will be discussed below, Applicant respectfully submits that claims 1, 4, 7, and 12 from which claims 2, 3, 5, 6, 8-11 and 13-17 depend now recite subject matter that is neither disclosed nor suggested by ***Maruyama*** or ***Dye***.

As shown and discussed, e.g., in Fig. 3 and on page 14 of the specification, the logical address requested by the CPU is compared with each of the logical addresses

stored in the logical address regions. Such comparisons are carried out in the comparators.

On the other hand, neither ***Maruyama*** nor ***Dye*** discloses, teaches or suggests such comparators for comparing logical addresses as now recited in claims 1-17.

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 1-17, and the prompt issuance of a Notice of Allowability are respectfully solicited.

If this application is not in better condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, Applicant hereby petitions for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2300. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300.

Respectfully submitted,

Arent Fox Kintner Plotkin & Kahn, PLLC

Raymond J. Ho
Attorney for Applicant
Registration No. 41,838

Customer No. **004372**
1050 Connecticut Avenue, N.W.
Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6000
Fax: (202) 638-4810
RJH/klf (#165636v1)
Enclosures: Marked-Up Copy of Claim Amendments

MARKED-UP COPY OF THE CLAIMS

1. (Twice Amended) A microprocessor to which a plurality of memory units having physical addresses different from each other are externally connected, said microprocessor comprising:

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memory units to a logical address of a load module stored in said first memory unit, wherein said load module includes instructions and data;

a copying unit which copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code copied to said second memory unit, wherein

said first address conversion unit comprises a first comparator that compares a requested logical address with said logical address assigned with said physical address of said first memory unit, and

said second address conversion unit comprises a second comparator that compares said requested logical address with said logical address assigned with said physical address of said second memory unit.

4. (Twice Amended) A microprocessor to which a plurality of memory units having physical addresses different from each other are externally connected, said microprocessor comprising:

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memory units to a logical address of a load module stored in said first memory unit, wherein said load module includes instructions and data;

a processing unit which temporarily stores and copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code stored in said second memory unit, wherein

said first address conversion unit comprises a first comparator that compares a requested logical address with said logical address assigned with said physical address of said first memory unit, and

said second address conversion unit comprises a second comparator that compares said requested logical address with said logical address assigned with said physical address of said second memory unit.

7. (Twice Amended) A memory device comprising:

a plurality of memory units having physical addresses different from each other;

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memories to a logical address of a load module stored in said first memory unit, wherein said load module includes instructions and data;

a copying unit which copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code copied to said second memory unit, wherein

said first address conversion unit comprises a first comparator that compares a requested logical address with said logical address assigned with said physical address of said first memory unit, and

said second address conversion unit comprises a second comparator that compares said requested logical address with said logical address assigned with said physical address of said second memory unit.

12. (Twice Amended) A memory device comprising:

a plurality of memory units having physical addresses different from each other;

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memory units to a logical address of a load module stored in said first memory unit, wherein said load module includes instructions and data;

a processing unit means which temporarily stores and copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code stored in said second memory unit, wherein

said first address conversion unit comprises a first comparator that compares a requested logical address with said logical address assigned with said physical address of said first memory unit, and

said second address conversion unit comprises a second comparator that compares said requested logical address with said logical address assigned with said physical address of said second memory unit.